Amendments to the Drawings:

The attached drawings include amendments to Figures 4-6 to correct minor infelicities. No new matter has been added.

Attachment: Replacement Sheets for Figures 1-6

REMARKS/ARGUMENTS

Claims 1-21 are pending in this application. The Final Office Action, dated January 27, 2006: rejected claims 1- 4, 13, and 15 – 20 under 35 U.S.C. § 102(b). Claims 5-9 are objected to. Claims 1, 5, 15, and 20 - 21 have been amended. No new subject matter has been added. For at least the following reasons, the Applicant respectfully submit that the pending claims as amended are in condition for allowance, and notice to that effect is requested.

It is requested that the present amendment be entered on the record along with the accompanying affidavit. The present amendment does not change the scope of the claims, and as such should not require further search for consideration. Previously presented claims and previously presented arguments that have already been entered on the record to identify various issues surrounding the interpretation that has been given on the record for the Gilbert reference (US Patent No. 5,077,541).

The present amendment was not previously presented since various terms used in the claims were expected to have been reasonably understood in those of skill in the relevant art. Applicant was made aware of certain interpretations that have been imparted to claim terms such as "offset", "null", "zero", "offset nulling", "band-gap", "band-gap core" and related terms from the present Final Office Action. Having only recently been made aware of the definition interpretation issues surrounding the claim terms, Applicant seeks to resolve any ambiguity with the present amendment and the accompanying affidavit. It is expected that entry of the present amendment places the application in condition for allowance.

Allowable Subject Matter

Claims 5 – 9 are objected to as being depending upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant wishes to thank the Examiner for the indication of allowable subject matter. Claim 5 has been amended to include the limitations of the base claim. Claims 6 through 9 depend upon and further limit claim 5, and should be allowable for at least that reason. Claims 5 - 9 are believed to be in proper form for allowance and notice to that effect is requested.

Claims 10 – 12 and 14 were indicated as including allowable subject matter in the prior Office Action dated September 14, 2005. Applicant filed a responsive amendment on December 14, 2005 that included an amendment to claims 10 and 14, which is believed to have addressed the issues for claims 10 – 12 and 14. The Final Office Action dated January 27. 2006 fails to address the status of claims 10 – 12 and 14. Since claims 10 – 12 and 14 have already been addressed in Applicant's remarks in the December 14, 2005 response, Applicant kindly refers the Examiner to the prior responsive submission. For those reasons previously presented, Applicant requests a notice of allowance for claims 10 – 12 and 14.

With respect to claim 21, the Final Office Action dated January 27, 2006 states that:

> Examiner has reconsidered the rejection to claim 21 and has accordingly removed such. The reference to Gilbert does not disclose the specific arrangement having 3 amplifiers and 3 offset adjustment circuit and wherein some "control signals" are "asserted" while others are "deasserted".

The same Final Office Action of January 27, 2006 states that claim 21 is rejected by the Gilbert reference under 35 U.S.C. § 102(b). It is believed that the rejection of claim 21 under 35 U.S.C. § 102(b) is an error, and that appropriate correction is requested. For the reasons

previously stated in the Applicant's December 14, 2005 response, claim 21 is believed to be in proper form for allowance. Based on the record stated above, it appears that the rejection of claim 21 based on the Gilbert reference is withdrawn, and a notice of allowance for claim 21 is requested.

Rejection of claims 1 - 4, 13 and 15 - 20 under 35 U.S.C. § 102(b)

Claims 1 - 4, 13, 15 – 19 and 21 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Gilbert* (U.S. Patent No. 5,077,541). Claims 1, 15, and 21 have been amended to clarify a distinction which was believed to be implicitly understood as part of the terms "band gap", and such claims are believed to be in condition for allowance. Claims 2 - 4, 13, and 16 - 19 depend upon and further limit claims 1 and 15 and are believed to be allowable for at least that reason.

The Office Action states that Gilbert discloses, in Figs. 3 and 4, a circuit comprising: "a first stage means (36) that includes an array of amplifier circuits (6)"; each amplifier including an offset adjustment circuit (I), a common node (inputs to 28)", and "an input (bases of 36)"; "a second stage means (28)";"a reference signal (SIGNAL OUTPUT)"; "a feedback means (feedback resistor, R, RT and resistor between 38 and RT)"; and "a null control means (Rs)". The Office Action further states that "Since the feedback arrangement would provide a band-gap operation, it would have been more than reasonable to consider the "feedback means" to be a "band-gap core circuit".

It is believed that the Office Action fails to present each of the claim limitations necessary to maintain a rejection under 35 U.S.C. § 102(b). Applicant's claim 1 as amended recites at least the following limitations that are not found in the cited prior art references:

> "a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit … arranged to remove a respective input referred offset for a respective one of the amplifier circuits … wherein each respective null control signal is independent of one another;"
>
> "a feedback circuit … wherein the feedback circuit includes a band-gap core circuit, wherein the band-gap core circuit comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE, wherein the first stage circuit, the second stage circuit, and the feedback circuit are arranged for closed-loop operation with the band-gap core circuit such that VBE1 = VBE2 + delta VBE;"
>
> "a null control logic circuit …"

Applicant's claim 15 as amended recites at least the following limitations that are not found in the cited prior art references:

> "a first amplifier means that includes a first offset adjustment circuit … the first offset adjustment circuit is arranged to remove a first input referred offset associated with the first amplifier means in response to the first null control signal;"
>
> "a second amplifier means that includes a second offset adjustment circuit … the second offset adjustment circuit is arranged to remove a second input referred offset associated with the second amplifier means in response to the second null control signal;"
>
> "a third amplifier means that includes a third offset adjustment circuit … the third offset adjustment circuit is arranged to remove a third input referred offset associated

with the third amplifier means in response to the third null control signal, wherein the first, second, and third null control signals are independent of one another"

"a feedback means ... wherein the feedback means includes a band-gap core means, wherein the band-gap core means comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE, wherein the first stage circuit, the second stage circuit, and the feedback circuit are arranged for closed-loop operation with the band-gap core means such that VBE1 = VBE2 + delta VBE;"

"a null control means ..."

Applicant's claim 21 as amended recites at least the following limitations that are not found in the cited prior art references:

"a feedback circuit ... includes a band-gap core circuit, wherein the band-gap core circuit comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE;"

"a null control logic circuit ...; and"

"an error amplifier circuit ... wherein the feedback circuit, the output circuit, and the error amplifier circuit are arranged for closed-loop operation with the band-gap core means such that VBE1 = VBE2 + delta VBE, wherein the error amplifier circuit comprises:"

"a first offset adjustment circuit that is integrally formed with the first amplifier circuit, wherein the first offset adjustment circuit is enabled in response to the first control signal;"

> "a second offset adjustment circuit that is contained within the second amplifier circuit, wherein the second offset adjustment circuit is enabled in response to the second control signal;"
>
> "a third offset adjustment circuit that is contained within the third amplifier circuit, wherein the third offset adjustment circuit is enabled in response to the third control signal, wherein: the feedback signal is coupled to one of the first and second nodes, and the other reference signal is coupled to an other of the first and second node, and the first, second, and third control signals are operated independent of one another;"

While the Applicant does not wish to re-iterate previously presented arguments, Applicant strongly urges the Examiner to reconsider the interpretation that "it would have been more than reasonable to consider the feedback means to be a band-gap core circuit". Moreover, for the Applicant strongly urges the Examiner to reconsider the interpretation that Gilbert discloses that each amplifier circuit includes "an offset adjustment circuit (I)" and a "null control means (R_S)".

First, the terms "band-gap", "band-gap core", "offset", "zero" and "null" have specific acceptable meanings that are understood within the relevant art. Second, the Gilbert reference does not describe, teach, or suggest, either explicitly or implicitly the use of a Band-Gap as is found in Applicant's claims 1, 15 and 21. Third, the Gilbert reference does not describe, teach, or suggest, either explicitly or implicitly the use of offset nulling in the amplifiers as is found in Applicant's claims 1, 15 and 21. As a result of these observations, it is believed that the Office Action does not identify every claimed feature of Applicant's claims 1, 15 and 21, which would be necessary to establish a case of anticipation. Moreover, the Office Action seems to suggest an

obviousness type rejection, which is equally inapplicable to Applicant's claims 1, 15 and 21. The discussion found below provides a detailed analysis of each of these issues.

"Band-Gap" has a Specific Acceptable Meaning in the Art

It is well understood in the art that the terms "band-gap", "band-gap core", and "band-gap circuit" have very specific meaning. The band-gap voltage of silicon has a value that is nominally 1.2V at 300 degrees Kelvin. **Every** circuit that is referred to as a **band-gap** is by design arranged to capitalize on the physical characteristics of the band-gap voltage to provide a temperature compensated output voltage.

It is notoriously well known in the art that the base emitter voltage of bipolar junction transistors or VBE has a negative temperature coefficient, while the thermal voltage or VT of a bipolar junction transistor has a positive temperature coefficient (VT = kT/q). **Every** band-gap circuit is arranged to provide an output voltage that is given by: VOUT = VBE + K*VT. Since VBE has a negative temperature coefficient and VT has a positive temperature coefficient, the output voltage can be made relatively independent of temperature by adjusting the value of K. It is notoriously well known in the art that the temperature stabilized output voltage for a band-gap circuit is equal to the band-gap voltage of silicon (for silicon based bipolar junction transistors) or 1.2V. The name "band-gap" is derived from this relationship, and has a well accepted meaning in the industry.

Every implementation of a "band-gap" **must** include the operation of two bipolar junction transistors (BJTs) and a resistive component in a very specific configuration. First, the

two BJTs **must** be arranged in a common base configuration. Second, the first BJT **must** be operated with a different current density than the second BJT. Third, the resistor **must** be series coupled to one BJT to measure a difference between the base-emitter voltages of the common-base BJTs, referred to as the delta VBE. Fourth, an amplifier circuit that is often referred to as an error amplifier **must** be arranged to adjust the operating currents of the two transistors so that the VBE of one transistor is equal to the sum of the VBE of the other transistor and the delta VBE. In other words, **every** "band-gap" circuit arrangement achieves a stable steady-state output voltage when VBE1 = VBE2 + delta VBE.

An affidavit from the inventor along with an information disclosure statement accompanies the response to this office action. A review of the affidavit with the supporting documents will reveal that the terms "band-gap", "band-gap circuit" and "band-gap core" and related terms have a well understood and accepted meaning within the industry. Moreover, the Applicant's specification and figures use such terms consistent within the acceptable meaning in the industry as is evidenced by, for example, FIGS. 4 – 6 and the supporting descriptions on: page 1, line 20 – page 2, line 8; page 4, lines 13 – 18; and page 8, lines 22 – 30.

<u>"Band-Gap" is Not Taught, Described, or Otherwise Suggested by Gilbert</u>

Although the Final Office Action states that "the feedback arrangement would provide a band-gap operation", there is no support in the Gilbert reference that teaches, describes or otherwise suggests anything related to a band-gap as is understood in the art. A text search of the Gilbert reference reveals that the terms "bandgap", "band-gap", "band gap", "bandgap voltage", "band-gap voltage", "band gap voltage", "bandgap reference", "band-gap reference",

"band gap reference", and other related terms are completely absent from the disclosure of Gilbert.

As described previously above, the term "band-gap" has a specific meaning as is understood by one of ordinary skill in the relevant art. The assertion in the Office Action that "the feedback arrangement would provide a band-gap operation" is flawed in that the feedback arrangement of Gilbert in fact does not provide band-gap operation. As identified above, the Gilbert reference does not even identify any terms relevant in the art for band-gap type circuits. The mere statement that a feedback circuit **could** be arranged for band-gap is speculative at best, and unsupported by the specification of Gilbert. Furthermore, the principals of operation for Gilbert are incompatible with band-gap operation in such a manner that only hindsight reconstruction reasoning could be used to cover the Applicant's invention as identified in Claims 1, 15 and 21. The principals of operation for Gilbert, and failed reasoning as to adapting the Gilbert reference for Band-gap operation are described further below.

Gilbert teaches "a variable gain amplifier including a ladder attenuator to which the input signal is applied" (e.g., see Abstract, and Col. 3 lines 13 – 25). The ladder attenuator is applied to the input signal, not the output signal. The ladder attenuator is formed by an R-2R ladder, which is well understood in the art. Resistor RT is a terminating resistor with a value equal to R for the resistor ladder circuit. The output signal (VO) of the amplifier taught in Gilbert (e.g., see. Col. 5, lines 41 – 65) is related to the input signal (VI) by a gain equation: VO = G*K*VI, where the input signal (VI) appears between the HI and LO terminals, G is the gain term, and K is the attenuator term from the ladder attenuator. Since resistors R and RT are part of the ladder

attenuator of Gilbert, the signals provided by them are ONLY related to the input signal applied across HI and LO. Since the ladder attenuator is NOT in the feedback loop of the amplifier, there is no practical way for the ladder attenuator to provide any type of band-gap operation. Although a ladder attenuator could potentially be placed into the feedback loop, doing so still does not result in band-gap operation. It is thus a complete enigma as to where Gilbert reference provides any suggestion, teaching, disclosure or motivation; either explicitly or implicitly to provide a band-gap operation as is described in Applicant's independent claims 1, 15 and 21.

Fig. 1 of Gilbert illustrates the block diagram for the operation of the detailed examples of Fig. 3 and Fig. 4. The resistor that is between 38 and resistor RT of Gilbert in Fig. 3 corresponds to the very same resistor illustrated as resistor Rf for Fig. 1. Resistor Rf of Fig. 1 is one of the gain setting resistors for what is commonly referred to as a non-inverting amplifier. The input signal (VI) is provided across the HI and LO terminals, where LO is the DC voltage reference or common-mode input voltage for the input signal (VI). This is further illustrated in Fig. 12 of Gilbert, where HI and LO are coupled to a voltage source labeled Vi between 22 and 24. It is well understood in the art that voltage sources ideally have zero input impedance. Since the resistor between 38 and resistor RT is connected at the LO terminal, which is decidedly for an input signal voltage source, there is NO feedback from the output of the amplifier to the junction of resistor 38 and resistor RT. In other words, resistors R and RT cannot provide feedback including a band-gap core as is described in Applicant's claims 1, 15 and 21.

For at least those reasons stated above, Applicant believes that the "band gap" described in Applicant's feedback circuit of independent claims 1, 15, and 21 are not found in the Gilbert

reference. Moreover, there is no inherent or explicit feature of the Gilbert reference that teaches, describes, or otherwise suggests the feedback operation of a bandgap that is found only in Applicants claims 1, 15 and 21. Applicant believes that a case for anticipation has not been clearly established, and that it is only through impermissible hindsight reconstruction that the Office Action arrives at an interpretation that Gilbert teaches a feedback arrangement that would provide a band-gap operation. Applicant requests that the rejection of claims 1 - 4, 13, 15 – 19 and 21 under 35 USC §102(b) be withdrawn, and a notice of allowance be provided.

Offset Nulling in an Amplifier has a Specific Acceptable Meaning in the Art

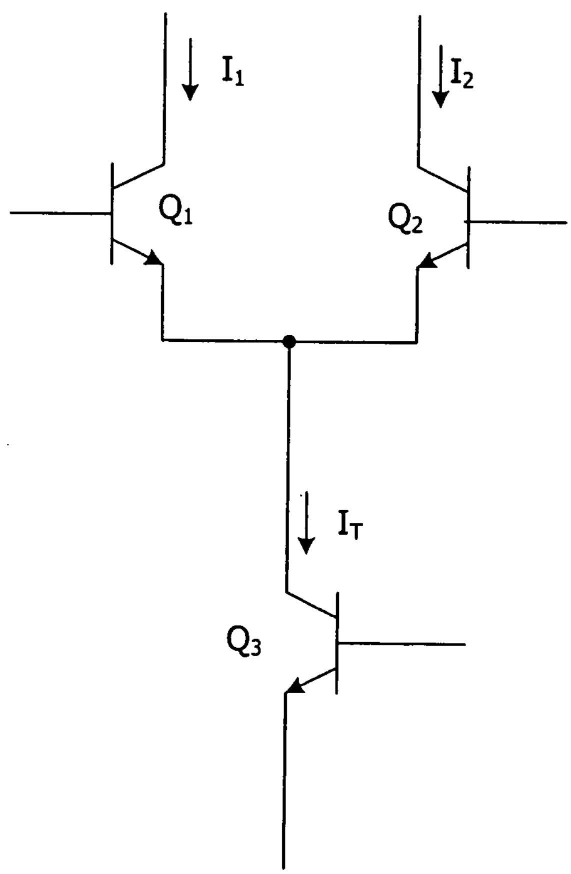
Although the present Office Action states that each amplifier includes "an offset adjustment circuit (I)", there is no support in the Gilbert reference that teaches, describes or otherwise suggests anything related to offset adjustment as is understood in the art. A text search of the Gilbert reference reveals that the terms "null", "nulling", "zero", "zeroing", "autozero", and "autozeroing", "offset removal", "offset canceling", "offset zeroing", "offset nulling" and other related terms are completely absent from the disclosure of Gilbert.

An affidavit from the inventor along with an information disclosure statement accompanies the response to this office action. A review of the affidavit with the supporting documents will reveal that the terms "null", "zero", "nulling" and "zeroing" and related terms have a well understood and accepted meaning within the industry when referring to "offset". Moreover, the Applicant's specification and figures use such terms consistent within the acceptable meaning in the industry as is evidenced by, for example, the descriptions on: page 3,

lines 15 – 18; page 5, lines 23 – 25; page 8, lines 1 – 5, and 13 – 18; page 9, lines 7 – 9; and page 10, lines .

"Offset Nulling" is Not Taught, Described, or Otherwise Suggested by Gilbert

The Gilbert reference describes gm stages that have use a differential pair of bipolar junction transistors (BJTs) that are arranged as follows:



Transistors Q_1 and Q_2 form a differential pair with a common emitter connection. The common emitter connection is connected to the collector of transistor Q_3, which is biased for operation as a current source to provide current I_T. When transistors Q_1 and Q_2 are perfectly

matched, and they are operated with identical input signals at their respective bases, there in no input referred offset for the amplifier. In other words, equally applied signals at the base of transistors Q_1 and Q_2 result in perfectly matched currents for I_1 and I_2, where $I_1 = I_2 = I_T/2$. An input referred offset occurs in this amplifier circuit when there is a mismatch between the emitter areas of transistors Q_1 and Q_2, or some other similar process derived mismatch.

Lets assume that there is an 10% mismatch between transistors Q_1 and Q_2 yielding a 10% difference in the currents. In this case, an additional biasing voltage will need to be applied to one of the transistors to match currents I_1 and I_2. The additional voltage that needs to be applied to the transistors is referred to as the input referred offset, which is a well understood and accepted term in the art. With equal base voltages for Q_1 and Q_2, $I_1 = (1.1)\, I_2$ and is given as:

$$I_1 = I_{S_1} e^{V_{BE_1}/V_{TH}}$$

$$I_2 = 1.1 I_{S_1} e^{V_{BE_2}/V_{TH}}$$

The voltage that needs to be applied between the inputs to match current I_1 to current I_2 is the offset voltage, which is given as $V_{OS} = V_{BE1} - V_{BE2}$. Dividing the above equations results in the following:

$$\frac{I_1}{I_2} = \frac{I_{S_1}}{1.1 I_{S_1}} e^{(V_{BE_1} - V_{BE_2})/V_{TH}}$$

When $V_{BE1} - V_{BE2} = V_{OS}$, currents I_1 and I_2 are matched ($I_1 = I_2$), yielding:

$$1.1 = e^{V_{OS}/V_{TH}}$$

Taking the natural log of both sides and rearranging the equations yields the following:

$$V_{OS} = V_{TH}\ln(1.1) = .026(.0953) = 2.47mV$$

In the above described example the offset voltage V_{OS}, is given as V_{TH} ln(1.1). However, the key observation is that the offset voltage (V_{OS}) is independent of the biasing current I_T. Instead, as illustrated by the above mathematical relationships, offset voltage is related to the current mismatch ratio (e.g., 1.1 for a 10% mismatch in the above example) and the thermal voltage (kT/q), both of which are independent of the current (I_T) provided by transistor Q_3. Thus, changing the bias current to the differential pair by adjusting the biasing of transistor Q_3 is not useful to adjust the offset voltage.

Now referring to at least Fig. 3 of Gilbert, we can observe that each gm stage (36) includes two transistors that are arranged as a differential pair, meaning that they have common-emitter connections with different base connections. The tail current source for this differential pair is represented as transistor 40. The bias current to transistor 40 in Figs. 3 and 4 of Gilbert is provided in part by current source I, and in part by any additional biasing current provided through resistor R_S. By varying the UP and DOWN control signals the total biasing current to transistor 40. Varying the biasing current to transistor 40 has the effect of varying the tail current (e.g. I_T) to the differential pair. However, varying the biasing current to a differential pair has no effect on the offset voltage as a consequence of the inherent characteristics of BJT based

differential pairs (see above analysis). In sum, varying the UP and DOWN control signals **cannot** be used to provide a deterministic effect on the offset voltage.

As previously stated the Office Action states that Gilbert teaches that each amplifier circuit includes "an offset adjustment circuit (I)" in Figs. 3 and 4 that are arranged in accordance with Applicant's claims 1, 15 and 21. For the above stated reasons, it is clear that adjustment of the current I does not yield any deterministic adjustment to offset voltage on the differential pair. Likewise, adjustment of the UP and DOWN control signals yields no deterministic adjustment to offset voltage.

For at least those reasons stated above, Applicant believes that the "offset adjustment circuit" as described in Applicant's independent claims 1, 15 and 21 are not found in the Gilbert reference. Moreover, there is no inherent or explicit feature of the Gilbert reference that teaches, describes, or otherwise suggests the offset adjustment that is found only in Applicants claims 1, 15 and 21. Applicant believes that a case for anticipation has not been clearly established, and that it is only through impermissible hindsight reconstruction that the Office Action arrives at an interpretation that Gilbert teaches an arrangement that would adjust offset for each amplifier in a manner consistent with Applicant's claims. Applicant requests that the rejection of claims 1 - 4, 13, 15 – 19 and 21 under 35 USC §102(b) be withdrawn, and a notice of allowance be provided.

Rejection of claim 20 under 35 U.S.C. § 102(b)

Claim 20 is rejected under 35 U.S.C. § 102(b) as being anticipated by *Gilbert* (U.S. Patent No. 5,077,541). Claim 20 is amended to clarify a minor point of distinction which was

believed to be implicitly understood as part of the terms "band gap", and is believed to be in condition for allowance.

The Office Action states that it is clearly reasonable to consider the cited elements as a band gap core, and that when one of transistors is turned off, it is reasonable to consider such to be nulled. The Office Action continues to state that offset of the amplifier circuit in Gilbert varies proportional to current, and that when tail current changes the "offset" will necessarily change in away that is the same as Applicant's claims.

It is believed that the Office Action fails to present each of the claim limitations necessary to maintain a rejection under 35 U.S.C. § 102(b). Applicant's claim 20 as amended recites at least the following limitations that are not found in the cited prior art references:

Applicant's claim 20 as amended recites at least the following limitations that are not found in the cited prior art references:

> "providing a feedback signal to the array of amplifier circuits ... wherein the feedback signal is associated with a band-gap core circuit, wherein the band-gap core circuit comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE;"
>
> "selecting one of the array of amplifier circuits for offline operation"
>
> "nulling an offset voltage associated with the selected amplifier circuit while the selected amplifier circuit is in offline operation"

> "controlling the non-selected amplifier circuits with the feedback signal for closed-loop operation with the band-gap core circuit such that VBE1 = VBE2 + delta VBE"
>
> "maintaining the non-selected amplifier circuits such that the offset voltage associated with the reference signal is zeroed as an average"

The reasoning utilized by the Office Action with respect to Claim 20 is extremely flawed and easily refuted by the scientific analysis previously provided above for the Gilbert reference. First, nothing in the Gilbert reference teaches a band-gap (see prior discussion above). Second, the terms "band-gap", "nulling" and "offset" as is conventionally used in the art are incompatible with the Office Action's suggested interpretation and contrary to the Applicant's specification (see prior discussions above). Third, the operation of the Gilbert reference cannot yield offset adjustment as is suggested in the Office Action (see prior discussion above).

For at least those reasons stated above with respect to claims 1, 15, and 21, Applicant believes that the features claimed in Applicant's independent claim 20 are not found in the Gilbert reference. Applicant believes that a case for anticipation has not been clearly established, and that it is only through impermissible hindsight reconstruction that the Office Action arrives at an interpretation that Gilbert teaches an arrangement that would utilize a band-gap core with an error amplifier for band-gap operation, where the error amplifier includes multiple amplifier circuits each with offset adjustment, in a manner consistent with Applicant's claim 20. Applicant requests that the rejection of claim 20 under 35 USC §102(b) be withdrawn, and a notice of allowance be provided.

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Respectfully submitted,

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